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Research Article

Embedded System for Real-Time Digital Processing of Medical Ultrasound Doppler Signals

S. Ricci, A. Dallai, E. Boni, L. Bassi, F. Guidi, A. Cellai, and P. Tortoli

Dipartimento Elettronica e Telecomunicazioni, Università degli Studi di Firenze, Via S. Marta 3, 50139 Firenze, Italy

Correspondence should be addressed to S. Ricci, stefanp.ricci@unifi.it

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Ultrasound (US) Doppler systems are routinely used for the diagnosis of cardiovascular diseases. Depending on the application, either single tone bursts or more complex waveforms are periodically transmitted throughout a piezoelectric transducer towards the region of interest. Extraction of Doppler information from echoes backscattered from moving blood cells typically involves coherent demodulation and matched filtering of the received signal, followed by a suitable processing module. In this paper, we present an embedded Doppler US system which has been designed as open research platform, programmable according to a variety of strategies in both transmission and reception. By suitably sharing the processing tasks between a state-of-the-art FPGA and a DSP, the system can be used in several medical US applications. As reference examples, the detection of microemboli in cerebral circulation and the measurement of wall „distension“ in carotid arteries are finally presented.

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1. INTRODUCTION

The well-known *Doppler effect* consists in the frequency shift of a wave, originated from the relative movement between the source and the receiver. In biomedical ultrasound (US) applications, such an effect is mainly exploited to perform blood flow velocity measurements, which are of interest for the diagnosis of cardiovascular diseases [1].

With reference to Figure 1, let us suppose having a single red blood cell (erythrocyte) moving with constant velocity, v , impinged by an acoustic plane wave of frequency f_0 . Let c be the speed of sound in the surrounding medium and δ the angle between the US propagation direction and the velocity vector of the target. Being $v \ll c$, the frequency shift between the transmitted and backscattered waves can be approximated by the following equation:

$$f_d = 2 \frac{f_0}{c} v \cos \delta. \quad (1)$$

By measuring the frequency shift f_d , it is possible to estimate the axial component, $v \cos \delta$, of the target velocity. The transmitted frequency, f_0 , used in most Doppler US applications ranges between 2 MHz and 10 MHz, to reach a few tens of MHz in specialized high-frequency equipment.

The expected blood velocities are typically lower than 1 m/s in the peripheral arteries of healthy subjects, with possible peaks of a few m/s in stenotic vessels [2]. Accordingly, the detected Doppler shift is generally in a range of a few kHz.

In order to reliably measure the frequency shifts caused by the movement of erythrocytes, both the transmit (TX) and receive (RX) sections of an US system must be suitably configured. In particular, in pulsed-wave (PW) Doppler systems, a short burst of US energy is transmitted during each pulse repetition interval (PRI). The transducer can be excited by either a single tone burst or a more complex signal produced by an arbitrary waveform generator (AWG). In some applications, for example, when US contrast agents are used [3] coded excitation strategies [4] are involved, while multiple arbitrary bursts are transmitted in elastographic studies [5]. Since each pulse is reflected/backscattered from all targets intercepted during US propagation, multiple echoes are received. The RX module typically includes in-phase quadrature (I/Q) demodulation, to allow the identification of (forward/reverse) flow direction through the base-band signal components. One or more sample volumes (SVs), that is, the spatial region which contributes to the echo received at a given time, can be explored by selecting, with suitable electronic “gates,” specific portions of the received

echo-signals. The gated Doppler signals are high-pass filtered to eliminate the “clutter,” that is, the high-level low-frequency components due to still or slowly moving targets like tissues or vessel walls. The clutter (whose amplitude can be 60 dB higher than the signal backscattered from blood) is generally removed because its presence could saturate the RX dynamic range. Finally, the frequency content of the filtered Doppler signal is estimated through either full spectral analysis or suitable mean frequency estimators.

In the last few years, all processing modules involved in Doppler systems have gradually migrated from analog to digital implementations. The availability of high-speed, high-resolution (12–14 bit) Analog-to-Digital (AD) converters now allows directly sampling the radio-frequency (RF) echo signal, according to the same approach followed in the so-called Software Defined Radio. This tendency is further encouraged by high-speed programmable devices such as digital signal processors (DSPs) and field programmable gate arrays (FPGAs), which have the calculation power requested to perform all needed processing in real time.

In this paper, an embedded system for multichannel multigate (MCMG) US echography is described. The system was conceived and realised as programmable research platform, capable of implementing arbitrary TX-RX strategies and user-defined processing. Section 2 reports details on how the processing load is shared between a floating point DSP and a single advanced FPGA so that the MCMG system can be used in a number of different applications. Two reference applications, the detection of microemboli in cerebral vessels and the assessment of wall distension in peripheral arteries, are presented in Section 3.

2. MCMG DIGITAL ARCHITECTURE

In the MCMG system, the basic tasks necessary to control the transmission of US bursts by a piezoelectric transducer and to extract the desired Doppler information from the received echoes are shared between two state-of-the-art programmable devices (see Figure 2): an FPGA from the Stratix family (Altera, San Jose, Calif) [6] and a DSP from the TMS320C67 family (Texas Instruments, Austin, Tex) [7].

Because of PW operation, two asynchronous and independent processes are involved. The first process is highly power demanding, as it includes TX burst generation, RX data acquisition, demodulation, and reordering, and must be performed within each PRI. The second process comprises the Doppler spectrum estimate and/or other processing tasks, which typically run with an independent rate which must be sufficient to produce a fluid result presentation (e.g., 50 fps). The former process mainly involves the FPGA and some direct memory access (DMA) channels in the DSP, while the latter is specific of remaining DMA channels and of the DSP core.

At the beginning of each PRI, the FPGA generates arbitrary TX waveforms, which are D/A converted at 64 Msps, amplified and sent to the US transducer (see Section 2.1). The received echoes are amplified with gain programmable in the range 20–60 dB, to fit the 14-bit A/D converter dynamics. The digital samples, obtained at 64 MHz, are

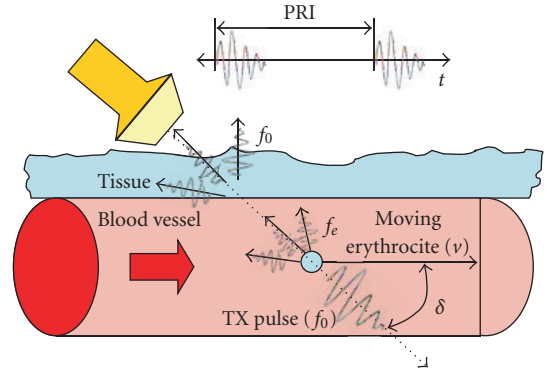


FIGURE 1: In PW Doppler investigations, an US pulse is transmitted into tissues during each PRI, causing echoes travelling back to the transducer carrying information about tissue interfaces and moving particles.

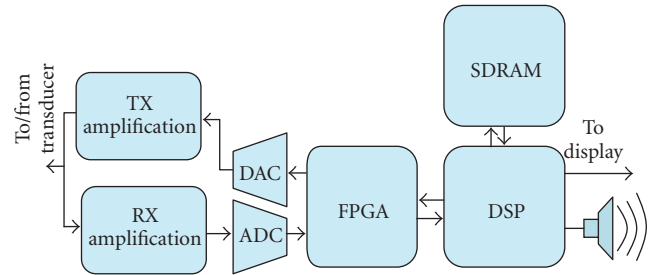


FIGURE 2: MCMG digital architecture.

coherently demodulated and low-pass filtered by the FPGA (see Section 2.2). The base-band and/or RF data are continuously stored in a large circular buffer by the DSP DMAs (see Section 2.3). This buffer is held inside a 64-MB SDRAM module, which represents the main system storage device. Other DMA channels are used to reorder the data collected in each PRI in a format suitable for subsequent processing. Finally, the DSP core produces an audio output (see Section 2.4) and processes the data according to the application specific algorithm which is selected in a suitable library. The processing results are sent through an USB 2.0 channel to a host PC where proprietary software is used to configure the MCMG system and for real-time display purposes. At any time, the acquisition can be stopped to download the data gathered in the circular buffer to the PC.

2.1. Arbitrary waveform generator

While in standard Doppler studies the transducer is excited by periodical single tone bursts, more complex excitation sequences are needed in some special applications [3, 4]. The MCMG system features an AWG based on a sequencer that executes a programmable code. The code contains the samples to be converted to analog, together with commands that control the sequence generation and the behaviour of related resources, such as the demodulator. The sequencer is implemented in the FPGA as a VHDL state machine which, at each clock cycle at 64 MHz, reads a word from the code

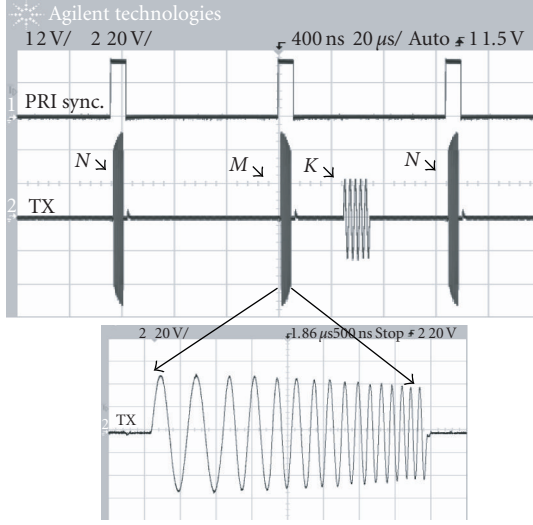


FIGURE 3: Oscilloscope acquisition of an excitation sequence involving 3 different waveforms over two consecutive PRIs. The bottom box shows the upward chirp signal on expanded scale. (PRI length ≈ 65 microseconds.)

stored in the internal memory, interprets the contents, and executes the command. The sequencer employs only 256 logic cells and one M-RAM [6] block to hold the code.

Complex sequences can be obtained by combining command-loops with synchronization instructions. Figure 3 (top) shows an example of TX sequence involving three different waveforms (N, M, K) over two consecutive PRIs. The oscilloscope channel 1 reports the PRI synchronism, while channel 2 shows the synthesised waveforms picked up at the output of the power amplifier. In the first PRI, a linear downward chirp (N) between 8 MHz and 2 MHz is fired, while every second PRI an upward chirp (M) symmetrical with respect to the previous one is generated. In the same PRI, a 0.5 MHz burst (K) of lower amplitude is also present.

The user can program the sequencer either directly or through a software that helps synthesising the TX waveforms through a graphical interface. A library of predefined configurations is available, and waveforms synthesized in different languages (e.g., Matlab) can be uploaded as well.

2.2. Coherent demodulation

In standard quadrature demodulation schemes, the demodulation frequency matches the TX frequency. However, as discussed above, in some cases multiple bursts having different centre frequencies are sequentially used. Moreover, in applications like harmonic Doppler imaging [8], the echo has to be demodulated by a multiple of the TX frequency. It can also be useful to simultaneously demodulate the same signal by different frequencies, to obtain, for example, the fundamental together with the harmonic component. An efficient and flexible architecture for digital coherent demodulation is thus requested.

In the MCMG system, 4 concurrent programmable coherent demodulators are fitted in the FPGA. The archi-

tecture of each demodulator is depicted in Figure 4. During each PRI, the demodulation quadrature signals are produced by a direct digital synthesizer (DDS) based on a 512-word look up table. Two 16-bit embedded multipliers process the input data stream to produce 32-bit results that feed two identical filtering channels. These include each a 4th-order cascaded-integrator-comb (CIC) filter, with a decimator between concatenated stages.

Each stage (see zoom-box in Figure 4) is based on a FIFO (64 words of 32 bit) and a 37-bit accumulator that prevents any possible saturation. The control logic produces the FIFO read signal (R) delayed by N -cycles with respect to the write signal (W), so that the FIFO acts as N stage shifter. Thus, the input of the accumulator register is

$$\text{Acc}(n) = \text{Acc}(n-1) + x(n) - x(n-N), \quad (2)$$

which represents a “recursive summing” architecture implementing a “moving averager.” Finally, the output sequence $y(n)$, after the decimator, is given by

$$y(n) = \sum_{i=0}^N x(Kn-i), \quad (3)$$

where N and K are the integration and decimation factors, respectively, which can be independently set for each CIC stage by the DSP.

Starting from the transfer function of a single comb filter in the Z domain, and taking into account the decimator blocks, through simple algebraic steps, the transfer function of the cascade can be written as

$$H(z) = \frac{1-z^{-N_1}}{1-z^{-1}} \cdot \frac{1-z^{-K_1N_2}}{1-z^{-K_1}} \cdot \frac{1-z^{-K_1K_2N_3}}{1-z^{-K_1K_2}} \cdot \frac{1-z^{-K_1K_2K_3N_4}}{1-z^{-K_1K_2K_3}} \quad (4)$$

the filter amplitude response can be finely tuned through the N values, to set the zero-transmission points over specific bands, like those crossing the demodulation image frequencies. Figure 5 shows an example. The transfer function of the filter has here been designed in order to reject by more than 100 dB a 500 kHz band centered at 4 MHz, when the TX and demodulation frequencies were both set at 2 MHz.

The demodulator output of each RX channel is finally converted to floating-point format and stored inside a 2 kB buffer.

Table 1 summarises the operations requested by the demodulation process. Each input sample is simultaneously multiplied by the in-phase/quadrature reference signal (2 multiplications). Each following CIC stage performs 3 sums (see (2)). Thus, assuming no decimation is performed, the complete demodulation process involves, for each input sample, 2 multiplications and 24 sums.

The use of CIC filters allowed saving multiplier units, thus making feasible fitting 4 demodulators in a single FPGA. Table 2 lists the FPGA resources requested for each demodulator. Each 16-bit multiplier employs 2 embedded DSP 9-bit elements. The right column of Table 1, in particular, reports the percent resources used in an EP1S10 Stratix device.

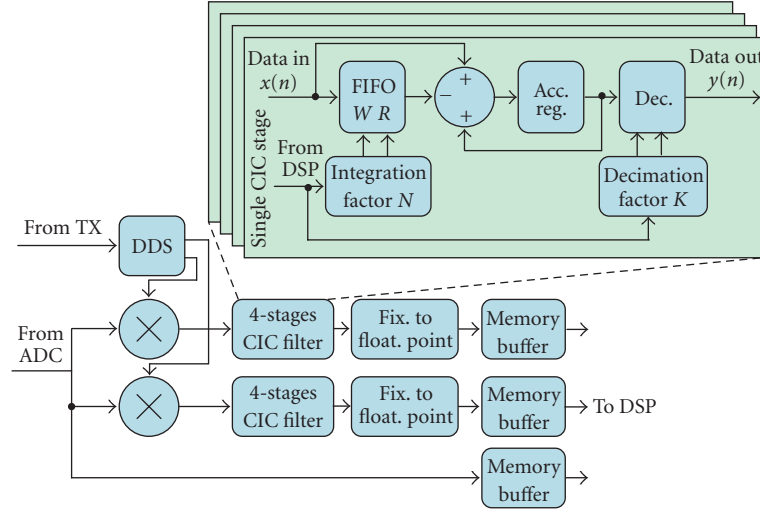


FIGURE 4: Architecture of coherent demodulators fitted in the FPGA. The zoom box reports details of each CIC filter stage.

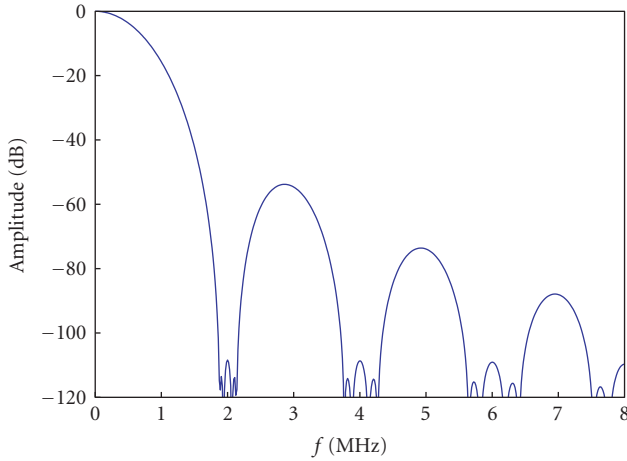


FIGURE 5: Example of CIC filter response.

2.3. Data managing and reordering

The main data bus of the MCMG system connects the FPGA, the DSP, and the memory bank through a 32-bit channel. The bus, mastered by the DSP, supports transfer rates up to 360 MB/s when communicating between the DSP and the SDRAM, and up to 90 MB/s when accessing the buffers inside the FPGA.

At each PRI, the DSP moves either the RF or the demodulated echo-data from the FPGA buffers to the SDRAM through two concatenated DMA channels. The whole memory space is managed as a circular buffer in order to store the latest acquired samples. This operation, for a typical PRI of 100 microseconds, produces a bus load of 30% of its maximum capacity.

Most algorithms coded in the DSP firmware needs, as data input, a vector of samples coming from the same depth over different PRIs. Hence, the DSP sorts the data read from the SDRAM according to the so-called “corner turning” (CT)

TABLE 1: Operations of the demodulator requested for each input sample.

	Multiplications	Sums
Multiplier	2	—
1 stage CIC	—	3
4-stage CIC—no decimation	—	12
Demodulation process	2	24

TABLE 2: Resource employed by a single demodulator.

	Employed resources	EP1S10
Memory bits	38512	4.2%
Embedded DSP 9-bit elements	4	8.3%
Logic cells	1688	16%

strategy, a term originally used in radar applications. The CT is equivalent to a matrix transposition. For instance, if we analyse 256 SVs by collecting data over 128 PRIs, the DSP has to transpose a matrix of 256×128 elements through 256 CTs of 128 elements each. The CT is performed by exploiting the sorting capabilities of the DMA channels, with no load for the DSP core. Once the vector with data regarding the same depth is ready into the internal DSP memory, an interrupt enables the core to start the specific processing (e.g., spectral analysis).

2.4. Audio processing

In vascular applications, the Doppler frequency shift spans the range 100 Hz–10 kHz. This range contains frequencies that humans can directly listen to, and, when properly trained, can use for diagnostic purposes. For this reason, most US Doppler instruments include an audio reproduction system. Depending on the flow direction respective to the US beam, the phase shift can be positive or negative, and

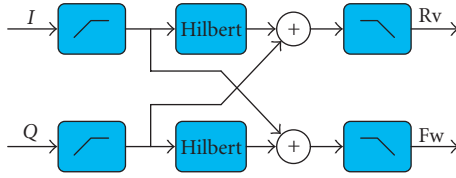


FIGURE 6: Forward/reverse splitter.

a forward/reverse extractor [9] allows distinguishing the two contributions in a stereo reproduction system.

The forward/reverse splitter scheme implemented in the MCMG system is illustrated in Figure 6. It is based on the Hilbert transform and is fed with the I/Q samples of a selected depth. In particular, the signal components laying on the negative band are shifted by $+90$ degrees, while those on the positive band are shifted by -90 degrees. In the forward channel, the negative band is suppressed, while the positive band is intact. Vice versa, the reverse channel contains only signal components covering the negative band.

The DSP implementation of the forward/reverse extractor is optimized in order to achieve accurate and fast processing. Accuracy is guaranteed by floating point calculations and by the large number of taps (127) of the FIR filter implementing the Hilbert transform. With such a filter, the undesired band in each output channel is attenuated by at least 50 dB over 95% of the band. Before the Hilbert transformer, a high-pass filter is inserted to attenuate the clutter (low frequency) components embedded in arterial wall and probe movements.

3. APPLICATION EXAMPLES

The flexibility of the MCMG system is here emphasised through two application examples. One regards the detection of micro-emboli in major cerebral arteries [10]. Their detection is of clinical interest since it is known that the majority of strokes are caused by emboli from distal sites, blocking vessels in the brain. A second application concerns the detection of arterial “distension,” that is, the arterial diameter changes in response to the pressure change produced during the cardiac cycle. This parameter is related to the elasticity of the arterial wall and has been proven to represent an important index for the early diagnosis of atherosclerotic diseases [11].

3.1. Detection of microemboli in cerebral vessels

The basic principle of emboli detection is quite simple: since an embolus is known to backscatter more power than the surrounding blood, its presence can be revealed by detecting the associate transient power increase. A major issue is represented by the need of distinguishing real embolic signals from artifacts due to, for example, transient noise or probe movements. This issue can be solved by analysing the Doppler signal simultaneously originated from different sites of the same vessel or from different vessels. For example,

a probe movement is expected to produce a simultaneous, similar effect on all detected signals, while a true embolic event would concern only the SVs placed at a specific location.

In this transcranial Doppler (TCD) application, the MCMG system was configured to contemporaneously analyse 4 SVs. A CT operation is here started every 4 milliseconds, instead of the typical 20 milliseconds, to produce output data at 250 fps. The samples collected in the most recent 128 PRIs from each selected SV are processed through 128-point FFTs, and the resulting power spectra are colour-coded and displayed in the classic spectrogram format [1]. Forward/reverse audio is calculated for each selected SV through the processing described above.

The MCMG system tracks the signal power to search for candidate embolic events. The trigger threshold is continuously calculated, using as idle power the value estimated for regions in which no event is detected. When an event is detected, 2 seconds of data around the event are stored. The software is arranged to manage several hours of continuous monitoring. After the end of the session, recorded data is processed through a neural network algorithm that, correlating the 4 available traces, selects the true embolic events.

In the test presented here, the probe was placed near the temporal bone of a patient, after informed consent was obtained. Due to the strong attenuation yielded by the passage of US through the skull, long bursts (>10 cycles) at low frequency (2 MHz) were transmitted to maintain an acceptable S/N ratio at the receiver. The RX bandwidth was accordingly reduced to hundreds of Hz, while the PRI was set in the range 200 microseconds-1 millisecond to make the analysis of deeply located SVs feasible.

Figure 7 shows a sample real-time window obtained by analysing the Doppler signals from SVs located at depths of 30 mm, 44 mm, 51 mm, 56 mm, respectively. The upper spectrogram is used as reference; the two central spectrograms intercept the same vessel, while the bottom one regards a second vessel producing a weak signal. An emboli candidate event, producing transient high power only in the central spectrograms, was detected at the time highlighted by arrows.

3.2. Measurement of wall “distension” in peripheral arteries

The physiologic maximum diameter change (distension) of carotid arteries during systole is of approximately $600\ \mu\text{m}$, about 10% of the diastolic diameter. Such a displacement, comparable to the US wavelength, is not easily detectable unless time-consuming 2D-autocorrelation techniques are used [12].

The procedure for measuring the distension starts by roughly locating the positions of the proximal and distal artery walls. This can be obtained by tracing the power peaks produced by the wall-blood discontinuity in the echo signal. Unfortunately, such a measurement is not accurate enough during all phases of the cardiac cycle. Thus, the signal from the two selected depths is correlated over subsequent PRIs to

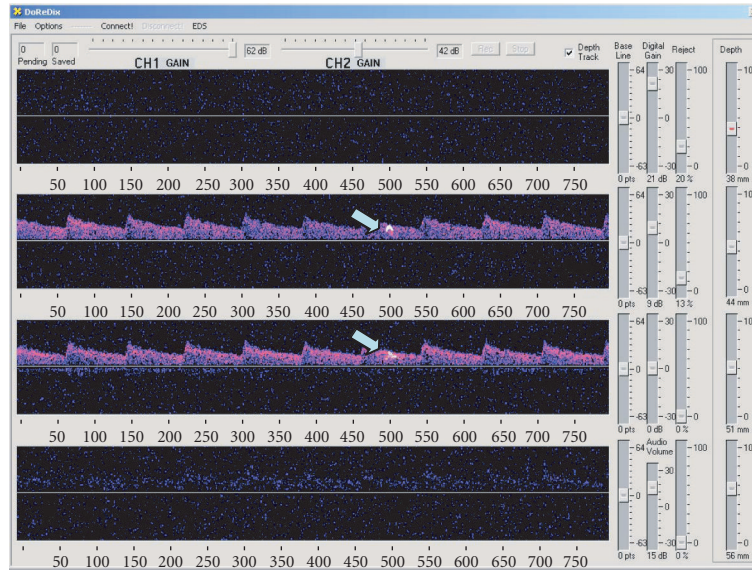


FIGURE 7: Display used in a 4-sonogram analysis implemented on the MCMG system for TCD applications. The arrows indicate a candidate embolic event detected at a depth of about 50 mm from the probe.

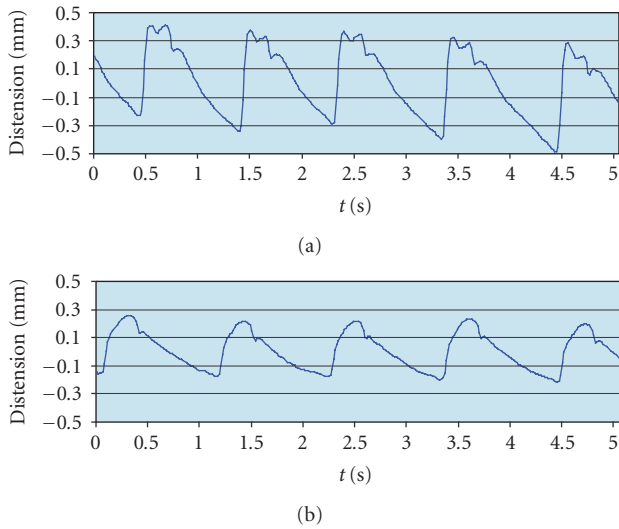


FIGURE 8: Distension waveforms measured in the carotid artery of two volunteers aged 31 (a) and 65 (b) featuring a distensibility of, respectively, 10% and 6%.

detect the local velocity, which is then integrated to calculate the relative displacement.

The aforementioned method was implemented in the DSP of the MCMG system and validated in [13]. Figure 8 reports the distension measured in the carotid artery of two female healthy volunteers, aged 31 and 65, respectively. The acquisitions, obtained with 200 microseconds PRI and a 5 MHz transducer, cover about 5 heart cycles in both cases, featuring a good repeatability among different subsequent cycles. In the younger volunteer (see Figure 8(a)), the carotid diameter is about 7 mm and thus the distensibility, that is, the maximum distension normalized with respect to the mean

vessel diameter) is 10%, while in the older the diameter is 7.5 mm and the distensibility results 6%. The diminished distensibility assessed in the older volunteer is a physiological effect of the reduced arterial elasticity typical of aging.

4. CONCLUSION

In this paper, an embedded system for real-time digital processing of US signals has been presented. The system is capable of transmitting arbitrary waveforms, simultaneously demodulating the echoes into multiple channels, and processing the received data through programmable algorithms. These features have been exploited in different applications such as emboli detection [14], characterization of contrast agents [15], arterial mechanics studies [16], and hemodynamic assessments [17]. The system implementation in a single electronic board makes it an ideal tool for any US research activity needing flexible transmission and reception strategies.

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In light of *Web 2.0*, The internet has become a user-generated multimedia content distribution medium for many different communities, including different types of video services: for example, YouTube, Apple Podcasts, or P2P video architectures like Joost. As the Internet is currently challenging many business cases for the provision of NGN communication services, it will also do so in the field of broadcasting and TV. There is no doubt that in the future NGN- and Web 2.0-enabled IPTV environments will be in a position to provide the required flexibility for supporting adequately the converged markets.

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thomas.magedanz@fokus.fraunhofer.de

Heinrich Arnold, Innovation Development Laboratory, Deutsche Telekom, Ernst-Reuter-Platz 7, 10587 Berlin, Germany; heinrich.arnold@telekom.de

Pete Distler, Sprint Mobile Media Network, 6220 Sprint Parkway, Overland Park, KS 66251, USA;
peter.distler@sprint.com

Ravi S. Sharma, Wee Kim Wee School of Communication and Information, Nanyang Technological University, 31 Nanyang Link, Singapore 637718; asrsharma@ntu.edu.sg

Special Issue on Patches in Vision

Call for Papers

The smallest primitive employed for describing an image is the pixel. However, analyzing an image as an ensemble of patches (i.e., spatially adjacent pixels/descriptors which are treated collectively as a single primitive), rather than individual pixels/descriptors, has some inherent advantages (i.e., computation, generalization, context, etc.) for numerous image and video content extraction applications (e.g., matching, correspondence, tracking, rendering, etc.). Common descriptors in literature, other than pixels, have been contours, shape, flow, and so forth.

Recently, many inroads have been made into novel tasks in image and video content extraction through the employment of patch-based representations with machine learning and pattern recognition techniques. Some of these novel areas include (but are not limited to):

- Object recognition/detection/tracking
- Event recognition/detection
- Structure from motion/multiview

In this special issue, we are soliciting papers from the image/video processing, computer vision, and pattern recognition communities that expand and explore the boundaries of patch representations in image and video content extraction.

Relevant topics to the issue include (but are not limited to):

- Novel methods for identifying (e.g., SIFT, DoGs, Harris detector) and employing salient patches
- Techniques that explore criteria for deciding the size and shape of a patch based on image content and the application
- Approaches that explore the employment of multiple and/or heterogeneous patch sizes and shapes during the analysis of an image
- Applications that explore how important relative patch position is, and whether there are advantages in allowing those patches to move freely or in a constrained fashion
- Novel methods that explore and extend the concept of patches to video (e.g. space-time patches/volumes)

- Approaches that draw upon previous work in structural pattern recognition in order to improve current patch-based algorithms
- Novel applications that extend the concept of patch-based analysis to other, hitherto, nonconventional areas of image and video processing, computer vision, and pattern recognition
- Novel techniques for estimating dependencies between patches in the same image (e.g., 3D rotations) to improve matching/correspondence algorithmic performance

Authors should follow the EURASIP Journal on Image and Video Processing manuscript format described at the journal site <http://www.hindawi.com/journals/ivp/>. Prospective authors should submit an electronic copy of their complete manuscripts through the journal Manuscript Tracking System at <http://mts.hindawi.com/>, according to the following timetable:

Manuscript Due	May 1, 2008
First Round of Reviews	August 1, 2008
Publication Date	November 1, 2008

Guest Editors

Simon Lucey, Robotics Institute, Carnegie Mellon University, Pittsburgh, PA, USA; slucey@ieee.org

Tsuhan Chen, ECE Department, Carnegie Mellon University, Pittsburgh PA, USA; tsuhan@cmu.edu

Special Issue on FPGA Supercomputing Platforms, Architectures, and Techniques for Accelerating Computationally Complex Algorithms

Call for Papers

Field-programmable gate arrays (FPGAs) provide an alternative route to high-performance computing where fine-grained synchronisation and parallelism are achieved with lower power consumption and higher performance than just microprocessor clusters. With microprocessors facing the “processor power wall problem” and application specific integrated circuits (ASICs) requiring expensive VLSI masks for each algorithm realisation, FPGAs bridge the gap by offering flexibility as well as performance. FPGAs at 65 nm and below have enough resources to accelerate many computationally complex algorithms used in simulations. Moreover, recent times have witnessed an increased interest in design of FPGA-based supercomputers.

This special issue is intended to present current state-of-the-art and most recent developments in FPGA-based supercomputing platforms and in using FPGAs to accelerate computationally complex simulations. Topics of interest include, but are not limited to, FPGA-based supercomputing platforms, design of high-throughput area time-efficient FPGA implementations of algorithms, programming languages, and tool support for FPGA supercomputing. Together these topics will highlight cutting-edge research in these areas and provide an excellent insight into emerging challenges in this research perspective. Papers are solicited in any of (but not limited to) the following areas:

- Architectures of FPGA-based supercomputers
 - History and surveys of FPGA-based supercomputers architectures
 - Novel architectures of supercomputers, including coprocessors, attached processors, and hybrid architectures
 - Roadmap of FPGA-based supercomputing
 - Example of acceleration of large applications/simulations using FPGA-based supercomputers
- FPGA implementations of computationally complex algorithms
 - Developing high throughput FPGA implementations of algorithms
 - Developing area time-efficient FPGA implementations of algorithms

- Precision analysis for algorithms to be implemented on FPGAs
- Compilers, languages, and systems
 - High-level languages for FPGA application development
 - Design of cluster middleware for FPGA-based supercomputing platforms
 - Operating systems for FPGA-based supercomputing platforms

Prospective authors should follow the EURASIP Journal on Embedded Systems manuscript format described at the journal site <http://www.hindawi.com/journals/es/>. Prospective authors should submit an electronic copy of their complete manuscript through the journal Manuscript Tracking System at <http://mts.hindawi.com/>, according to the following timetable:

Manuscript Due	July 1, 2008
First Round of Reviews	October 1, 2008
Publication Date	January 1, 2009

Guest Editors

Vinay Sriram, Defence and Systems Institute, University of South Australia, Adelaide, South Australia 5001, Australia; vinay.sriram@unisa.edu.au

David Kearney, School of Computer and Information Science, University of South Australia, Adelaide, South Australia 5001, Australia; david. Kearney@unisa.edu.au

Lakhmi Jain, School of Electrical and Information Engineering, University of South Australia, Adelaide, South Australia 5001, Australia; lakhmi.jain@unisa.edu.au

Miriam Leeser, School of Electrical and Computer Engineering, Northeastern University, Boston, MA 02115, USA; mel@coe.neu.edu

Special Issue on Wireless Physical Layer Security

Call for Papers

Security is a critical issue in multiuser wireless networks in which secure transmissions are becoming increasingly difficult to obtain in highly mobile and distributed environments. In his seminal works of the late 1940s, Shannon formalized the concepts of capacity (as a transmission efficiency measure) and equivocation (as a measure of secrecy). Together with Wyner's fundamental formulation of the wiretap channel in the 1970s, this work laid the groundwork for the area of wireless physical layer security. Interest in this area has exploded in recent years, motivated by the rise of wireless networking in general and by the increasing interest in large mobile networks with light infrastructure, which are extremely difficult to secure by traditional methods.

The objective of this special issue (whose preparation is carried out under the auspices of the EC Network of Excellence in Wireless Communications NEWCOM++) is to gather recent advances in the area of wireless physical layer security from the theoretical, such as the analysis of the secrecy capacity of various channel models, to more practical interests such as the development of codes and other communication schemes that can provide security in real networks. Suitable topics for this special issue dedicated to physical layer security include but are not limited to:

- Opportunistic secrecy
- The wiretap channel with feedback
- Authentication over the wiretap channel
- Information theoretic secrecy of fading channels
- Secrecy through public discussion
- Wireless key distribution
- Multiuser channels with secrecy constraints
- MIMO wiretap channels
- Relay-eavesdropper channel
- Scheduling for secure communications
- Secure communication with jamming
- Game theoretic approaches for secrecy
- Codes for secure transmission
- Secure compression
- Cognitive approaches for secrecy
- Physical Secrecy and Common Randomness
- Secrecy with channel uncertainty

Authors should follow the EURASIP Journal on Wireless Communications and Networking manuscript format described at the journal site <http://www.hindawi.com/journals/wcn/>. Prospective authors should submit an electronic copy of their complete manuscript through the journal Manuscript Tracking System at <http://mts.hindawi.com/>, according to the following timetable.

Manuscript Due	October 1, 2008
First Round of Reviews	January 1, 2009
Publication Date	April 1, 2009

Guest Editors

Mérouane Debbah, Alcatel-Lucent Chair on Flexible Radio, Supélec, 3 rue Joliot-Curie, 91192 Gif-sur-Yvette Cedex, France; merouane.debbah@supelec.fr

Hesham El-Gamal, Department of Electrical & Computer Engineering, Ohio State University, 205 Drees Labs, 2015 Neil Avenue Columbus, OH 43210, USA; helgamal@ece.osu.edu

H. Vincent Poor, Department of Electrical Engineering, Princeton University, Engineering Quadrangle, Olden Street, Princeton, NJ 08544, USA; poor@princeton.edu

Shlomo Shamai, Department of Electrical Engineering, Technion, Technion City, Haifa 32000, Israel; sshlomo@ee.technion.ac.il

Special Issue on Secure Steganography in Multimedia Content

Call for Papers

Steganography, the art and science of invisible communication, aims to transmit information that is embedded invisibly into carrier data. Different from cryptography it hides the very existence of the secret. Its main requirement is undetectability, that is, no method should be able to detect a hidden message in carrier data. This also differentiates steganography from watermarking where the secrecy of hidden data is not required. Watermarking serves in some way the carrier, while in steganography, the carrier serves as a decoy for the hidden message.

The theoretical foundations of steganography and detection theory have been advanced rapidly, resulting in improved steganographic algorithms as well as more accurate models of their capacity and weaknesses.

However, the field of steganography still faces many challenges. Recent research in steganography and steganalysis has far-reaching connections to machine learning, coding theory, and signal processing. There are powerful blind (or universal) detection methods, which are not fine-tuned to a particular embedding method, but detect steganographic changes using a classifier that is trained with features from known media. Coding theory facilitates increased embedding efficiency and adaptiveness to carrier data, both of which will increase the security of steganographic algorithms. Finally, both practical steganographic algorithms and steganalytic methods require signal processing of common media like images, audio, and video. The field of steganography still faces many challenges, for example,

- how could one make benchmarking steganography more independent from machine learning used in steganalysis?
- where could one embed the secret to make steganography more secure? (content adaptivity problem).
- what is the most secure steganography for a given carrier?

Material for experimental evaluation will be made available at <http://dud.inf.tu-dresden.de/~westfeld/rsp/rsp.html>.

The main goal of this special issue is to provide a state-of-the-art view on current research in the field of steganographic applications. Some of the related research topics for the submission include, but are not limited to:

- Performance, complexity, and security analysis of steganographic methods

- Practical secure steganographic methods for images, audio, video, and more exotic media and bounds on detection reliability
- Adaptive, content-aware embedding in various transform domains
- Large-scale experimental setups and carrier modeling
- Energy-efficient realization of embedding pertaining encoding and encryption
- Steganography in active warden scenario, robust steganography
- Interplay between capacity, embedding efficiency, coding, and detectability
- Steganalytic application in steganography benchmarking and digital forensics
- Attacks against steganalytic applications
- Information-theoretic aspects of steganographic security

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Publication Date	February 1, 2009

Guest Editors

Miroslav Goljan, Department of Electrical and Computer Engineering, Watson School of Engineering and Applied Science, Binghamton University, P.O. Box 6000, Binghamton, NY 13902-6000, USA; mgoljan@binghamton.edu

Andreas Westfeld, Institute for System Architecture, Faculty of Computer Science, Dresden University of Technology, Helmholtzstraße 10, 01069 Dresden, Germany; westfeld@inf.tu-dresden.de

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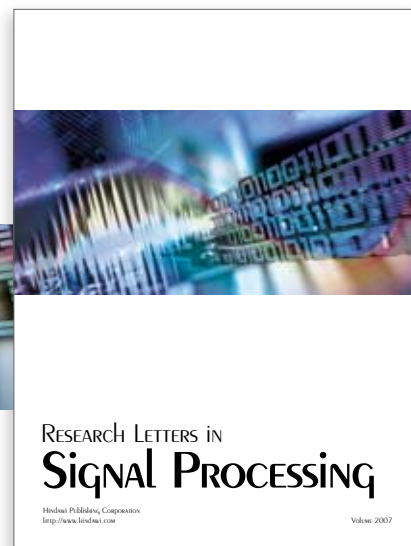
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